ABSTRACT OF THE DISCLOSURE

A semiconductor memory device includes memory cells each having a trench capacitor and a fin-gate-type MOSFET that selects the trench capacitor. One of activation regions of the MOSFET, which are provided in a pillar, and one of electrodes of the trench capacitor are electrically connected by a surface strap. The surface strap contacts an upper surface and an upper part of a side wall of the pillar.